Properties of the Low-Temperature Polycrystalline Silicon Film on Bottom Gate Electrode by Using Yttria-Stabilized Zirconia Stimulation Layer and Solid Phase Crystallization Methods

Mai Lien Thi Kieu, Kazuhide Mochizuki, and Susumu Horita

School of Materials Science, Japan Advanced Institute of Science and Technology, 1-1 Asahidai, Nomi, Ishikawa, 923-1291, Japan

Abstract

We successfully obtained a polycrystalline silicon (poly-Si) film at low temperature by using yttria-stabilized zirconia (YSZ) stimulation layer combined with solid phase crystallization (SPC) methods. Gate insulator capability of YSZ layer was also investigated by electrical properties (C-V, I-V) measurements.

1. Introduction

In the last several decades, thin film transistors (TFTs) have been much attractive for using as switching devices in active matrix flat panel displays (AM-FPD) [1]. Among many channel materials, polycrystalline silicon (poly-Si) TFTs have great advantages of stability, higher reliability, and mobility [2-4]. In order to satisfy the demands for low cost and high performance, for low-temperature fabrication process of poly-Si film, several crystallization methods of amorphous silicon (a-Si) films have been reported, such as solid phase crystallization (SPC) [5-7], metal-induced lateral crystallization (MILC) [8-10], pulse laser annealing (PLA) [11-15], and so on. However, these methods have their own disadvantages such as high process temperature and long annealing time (SPC), remnant metal as a leakage current source (MILC), expensive system, high surface roughness of fabricated films, and non-uniformity of grain size (PLA), etc.

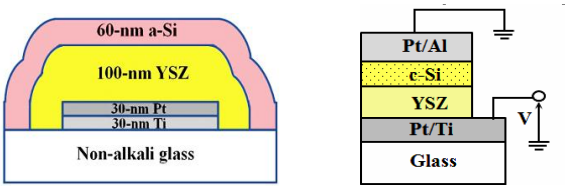
Therefore, in order to solve these problems, we have proposed a stimulation layer method using yttria-stabilized zirconia [$(ZrO_2)_{1-x}(Y_2O_3)_x$: YSZ] as a stimulation material [16]. Since YSZ has the small lattice mismatch and same cubic crystal structure with Si, it can be expected that an obtained poly-Si film has uniform grain size and crystallographic orientation. However, our previous research found that direct deposition of Si on a YSZ layer was unsuitable for TFT applications due to high surface roughness of the crystallized Si film and impurity of zirconium (Zr) diffusion into the Si film from the YSZ layer although the deposition temperature for crystallization was actually lower by 100^0C than that without a YSZ layer [17]. To limit these drawbacks, we used the SPC method in combination with a YSZ stimulation layer. Actually, it was found that SPC time of a-Si film on the YSZ layer was reduced compared with that without one [18, 19]. Also, the Si surface roughness and the Zr diffusion were reduced significantly.

In this meeting, we report the crystallization of a-Si films on metal films by SPC combined with YSZ stimulation layer methods and poly-Si electrical properties estimated by C-V and I-V measurements. Through the results, we discuss whether the YSZ layer is proper for a gate insulator or not.

2. Experimental

A fabricated sample structure is shown in Fig. 1. First, a non-alkali glass substrate is chemically cleaned before the deposition of gate electrode layers by sputtering method at deposition temperature of 100 ^{o}C. Pt and Ti are chosen as materials for gate electrode. Then, a YSZ stimulation layer is deposited at substrate temperature of 50 ^{o}C by reactive magnetron sputtering with Ar and O_2 as sputtering and reactive gases, respectively. The sputtering target is a 99.9% Zr metal target, on which eight pieces of 1x1 cm^2 99.9% Y pellets are placed in a circular arrangement [20]. To remove a contaminated and damage layer on surface of the YSZ, the sample is dipped in a diluted 5% HF solution in 3 min [14] prior to an a-Si film deposition by e-beam evaporation method at 300 ^{o}C using a-Si:B doped pellet of $5x10^{17}/cm^3$ in concentration as a source. Subsequently, crystallization of a-Si film is performed on YSZ/Pt/Ti layer by SPC method with crystallization temperature of 560 ^{o}C. The crystallization degree of Si films is estimated by Raman spectroscopy. The crystalline fraction, X, is determined by: $X = \left(I_\mu + I_c\right) / \left(I_\mu + I_c + I_a\right)$, where I_c, I_μ, and I_a are integrated intensities of crystalline silicon (c-Si), micro-crystalline silicon (μ-Si), and a-Si peaks, respectively [21]. For electrical measurement, bottom electrodes of 200-μm-diameter circles are formed on island-etching crystallized Si

films. Finally, the fabricated sample is post-annealed in nitrogen (N_2) ambient at 200 ^oC for 30 min prior to C-V and I-V measurements.



(a) (b)

Fig. 1 (a) Schematic annealed sample structure and (b) electrical measurement sample structure.

3. Results and discussions

Figures 2 (a), (b), and (c) show the Raman spectra of Si/glass, Si/YSZ/glass, and Si/YSZ/metal/glass regions, respectively.

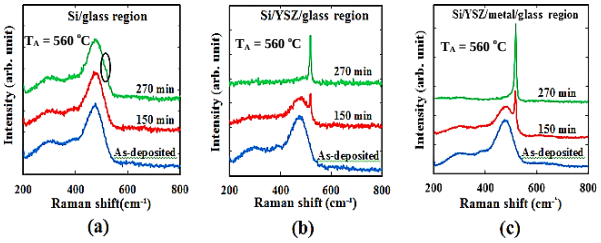


Fig. 2 Raman spectra of (a) Si/glass region, (b) Si/YSZ/glass region, and (c) Si/YSZ/metal/glass region.

It can be seen that sharp c-Si peaks at about 517 cm^{-1} appear only after 150 min annealing for Si films deposited on YSZ layers (Figs. 2 (b) and (c)) while a very small c-Si peak together with a broad a-Si peak at about 480 cm^{-1} appear on Si/glass region after 270 min annealing (Fig. 2 (a)). This means that the Si films deposited on YSZ layers are crystallized faster than that directly on non-alkali glass, which indicates the stimulating effect of YSZ layer. Moreover, the crystallization of a-Si on YSZ/metal/glass region is faster than that of YSZ/glass region. This is probably due to the gate electrode layer, which absorbs optical or thermal energy from the furnace, so that temperature of the Si film is a little higher than that in the non-metal region. This small temperature rising maybe enhance crystallization of a-Si after consecutive annealing process.

Figure 3 shows the dependences of crystalline fraction X on the annealing time t_A for Si/YSZ/metal/glass, Si/YSZ/glass, and Si/glass regions. Comparing 3 dependences, we can clearly see that a-Si on YSZ layers start to crystallize earlier than that directly on glass. It can also be seen that X of Si/YSZ/glass region increases almost linearly with t_A. This means that crystallization of a-Si proceeds from the interface of YSZ/a-Si. However, the dependences of Si/YSZ/metal/glass and Si/glass regions are non-linear with t_A.

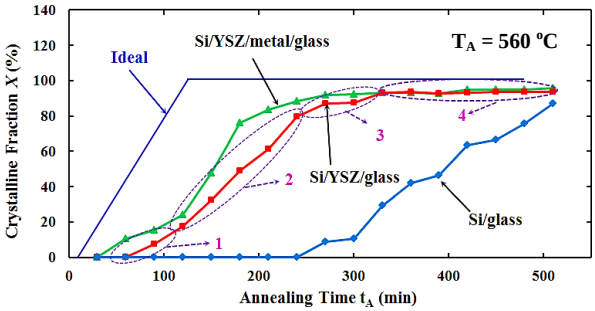


Fig. 3 Dependences of the crystalline fraction X on the annealing time t_A.

Now, we focus on the crystalline fraction of Si/YSZ/glass region. Ideally, the crystallization of a-Si film by SPC method in combination with the YSZ stimulation layer shows one linear region and one saturation region as shown in Fig. 3. The linear region begins from the nucleation of c-Si clusters, and continues with the progress of crystallization of a-Si region. The saturation region corresponds to completion of a-Si crystallization. However, the experimental result shows non-linear regions indicated by label 1 and 3 in Fig. 3 as well as linear and saturation regions (label 2 and 4). An illustration for the crystallization growth of a-Si film is shown in Fig. 4. The nucleation of poly-Si clusters, which is expected to start at the interface between YSZ layer and a-Si film, is non-uniform with grain size of $\sim 15nm$ (Fig. 4(1)). However, the spot size of Raman spectroscopy is $\sim 1\mu m$ in diameter, which is much larger than grains size. Therefore, the repeated measurement points cannot be exactly the same. This is considered to be one of the reasons for non-linear regions in Fig. 3.

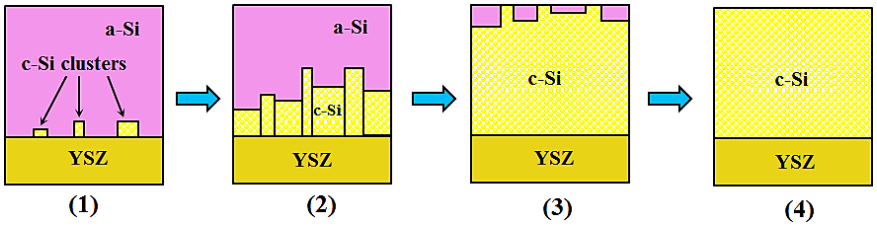


Fig. 4 Illustrations for the crystallization growth of a-Si on YSZ stimulation layer.

When c-Si clusters in the remained a-Si at the interface have reached the critical sizes, all of a-Si region near the interface become crystallized and the crystallized region grows or go up along the vertical direction (Fig. 4(2)). This is thanks to crystalline information of the stimulation YSZ layer. Therefore, the crystalline fraction of this state increases linearly, corresponding to the region 2 in Fig. 3. After almost c-Si clusters impinge each other, there is a transition (Fig. 4(3)) between linear and saturation (Fig. 4(4)) states, i.e., region 3 in Fig. 3 instead of the instantaneous transition as ideal case. The non-linear dependence of *X* on t_A in Si/YSZ/metal/glass might be due to the contaminants absorption in this region. For Si/glass region, the reason for non-linear dependence seems to be related with random nucleation in the a-Si film.

The C-V characteristics of the (Ti/Pt)/YSZ/c-Si/(Al/Pt) structure at various frequencies are shown in Fig. 5 with the sweep rate of 0.2 V/s. C_o in this figure is defined as the measurement capacitance at gate voltage V of -10 V for each frequency. The inset shows the C-V curves with the full range of capacitance C/C_o.

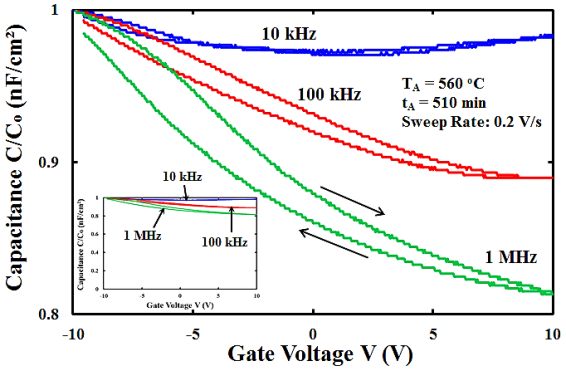


Fig. 5 C-V curves of a (Ti/Pt)/YSZ/c-Si/(Al/Pt) capacitor.

We can see p-type C-V curves with accumulation and depletion regions together with their frequency dependences. This is probably due to the B doped Si evaporation source although actual B concentration in the crystallized film has not been measured yet. From the C-V curves, it can be said that the gate voltage controls free carriers at the interface. However, the transitions from accumulation to depletion regions and vice versa are not so clear due to high interface trap. Further, at lower frequency of 10 kHz compared with 1 MHz and 100 kHz, formation of strong inversion can be observed at gate voltage larger than about 4 V. However, the ratio between accumulation and depletion capacitances is much lower than ideal bulk MOS case, which is more clearly shown from the inset. This phenomenon seems something strange, compared with the ideal MOS case, and can be considered as follows.

If the capacitance at V = 10 V is a series capacitance of YSZ layer and Si depletion layer, the depletion layer thickness can be estimated to be about 14 nm from the accumulation capacitance of 163 nF/cm^2 at V = -10 V and at 1 MHz. This estimated thickness is much smaller than the deposited thickness of 60 nm. From this, it can be considered that the crystallized Si film is so defective and the depletion region for positive gate voltage is not perfectly formed. This means that the c-Si layer in this case acts as a lower resistor or non-ideal depleted layer for the movement of free carriers from (Pt/Al) electrode to YSZ layer. So, due to large leakage current through the depletion layer, the depletion capacitance is much larger compared with that estimated one from the deposition thickness. Also, due to the same reason, the increase of depletion capacitance at positive gate voltage occurs at relatively higher frequency of 10 kHz compared with that lower than 1 kHz for ideal MOS case. It also can be observed ion drift hysteresis, which is due to mobile ions in YSZ layer. These mobile ions are probably H^+ and oxygen vacancies. During the cleaning process with water, ions H^+ in water can combine with ion O^{2-} in YSZ layer. Under the high temperature heating, this bond is broken and mobile ions H^+ are produced. There are some reports that the oxygen vacancies in YSZ layer also move under electric field [22, 23].

The I-V characteristics of the (Ti/Pt)/YSZ/c-Si/(Al/Pt) structure are shown in Fig. 6. From this figure, relatively low leakage current densities (lower than $1x10^{-7}A/cm^{-2}$) are observed for both the polarities of gate voltage. This means that YSZ is seemed to be a good gate insulator.

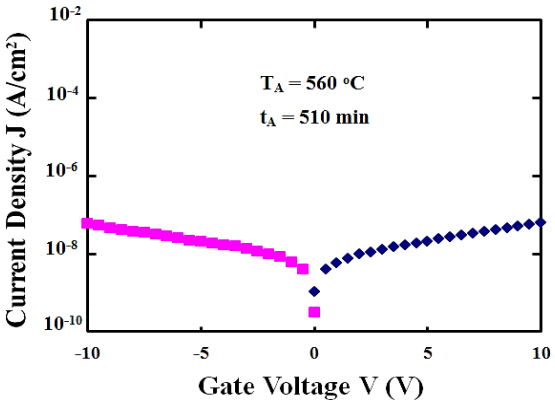


Fig. 6 J-V curves of a (Ti/Pt)/YSZ/c-Si/(Al/Pt) capacitor.

4. Conclusion

We have tried to fabricate and crystallize a-Si films by using SPC method and a stimulation layer of YSZ. It was found that the a-Si film was successfully crystallized from the YSZ interface and the stimulating effect of YSZ is operative on a-Si/YSZ/metal/glass structure. We also discussed the annealing results. It can be concluded that the crystallization of an a-Si film on a metal layer as bottom electrode by using the YSZ stimulation layer in combination with the SPC method is proved to be acceptable for TFT fabrication. The C-V characteristics of (Ti/Pt)/YSZ/c-Si/(Al/Pt) structure show that gate voltage can control free carriers at the interface between the YSZ layer and the c-Si film. A relatively low leakage current was shown from I-V characteristics. This means that the YSZ layer is believed to work as a comparatively good gate insulator.

References

[1] Emi Machida et al., Report AM-FPD **12** Conference, 2012, P-9.

[2] T. Sameshima, S. Usui, and M. Sekiya, IEEE Electron Device Letters **7**, (1976) 276-278.

[3] S. Uchikoga and N. Ibaraki, Thin Solid Films **383**, (2001) 19.

[4] Y. W. Choi, J. N. Lee, T. W. Jang, and B. T. Ahn, IEEE Electron Device Letters **20**, (1999) 2-4.

[5] K. Pangal, J. C. Sturm, S. Wagner, and T. H. Buyuklimanli, J. Appl. Phys. **85** (1999) 1900.

[6] R Kakkad, J. Smith, W. S. Lau, S. J. Fonash, and R Kerns, J. Appl. Phys. **65**, (1989) 2069.

[7] Gang Liu and S. J. Fonash, Appl. Phys. Lett. **55**, (1989) 660.

[8] R. C. Cammarata, C. V. Thompson, C. Hayzelden and K. N. Tu, Journal of Material Research **5**, (1990), 2133-2138.

[9] Soo Young Yoon, Ki Hyung Kim, Chae Ok Kim, Jae Young Oh, and Jin Jang, J. Appl. Phys. **82**, (1997) 5865.

[10] G. Radnoczi, A. Robertsson, H. T. G. Hentzell, S. F. Gong, and M.-A. Hasan, J. Appl. Phys. **69**, (1991) 6394.

[11] Norbert H. Nickel, "Laser crystallization of silicon", volume **75**, Elsevier 2003.

[12] R. A. Lemons, M. A. Bosch, A. H. Dayem, J. K. Grogan, and P. M. Mankiewich, Appl. Phys. Lett. **40**, (1982) 469.

[13] T.E. Dyer, J.M. Marshall, W. Pickin, A.R. Hepburn and J.F. Davies, Journal of Non-Crystalline Solids **164-166** (1993) 1001-1004.

[14] T. Sameshima, M. Hara, and S. Usui, Jpn. J. Appl. Phys. **28** (1989) L2131-L2133.

[15] John C. C. Fan and H. J. Zeiger, Appl. Phys. Lett. **27**, (1975) 224.

[16] S. Horita, K. Kanazawa, K. Nishioka, K. Higashimine, and M. Koyano, Mater. Res. Soc. Symp. Proc. **910** (2006) 0910-A21-17.

[17] S. Horita and S. Hana, Jpn. J. Appl. Phys. **49** (2010) 105801.

[18] S. Hana, T. Akahori, and S. Horita: Proc. 16th Int. Display Workshops, 2009 (IDW 09), FMC1-1, p. 271.

[19] S. Horita and T. Akahori: Abst. (7th Annual Meet. 2010); Thin Film Materials & Devices Meeting, 6P12 [in Japanese].

[20] S. Hana and S. Horita, Thin Solid Films **517** (2009) 5830.

[21] S. Ray, S. Mukhopadhyay, T. Jana, and R. Carius, Journal of Non-Crystalline Solids **299–302,** (2002) 761–766.

[22] S. Horita, M. Watanabe, and A. Masuda, Materials Science and Engineering **B54**, (1998) 79-83.

[23] S. Horita, H. Nakajima, and T. Kuniya, Vacuum **59**, (2000) 390-396.